IN THE CLAIMS

This version of the claims replaces and supercedes all prior versions of the claims.

1. – 19. (Canceled)

20. (Withdrawn) A computer-readable recording medium on which is recorded a program for causing a computer to execute designing a system LSI circuit having a plurality of processor functions for executing a plurality of instruction sets, said program comprising:

(a) dividing system LSI circuit design specifications into hardware design and software design at a function designing stage;

(b) receiving, in hardware design, as hardware information, hardware configurations corresponding to respective ones of the plurality of processors, and the system instruction and the plurality of instruction sets described at an algorithm level; and

(c) performing behavioral synthesis using the hardware information, wherein said processor includes:

a system instruction decoder, provided separately of the plurality of processor functions, for decoding a system instruction that is not executed by any of the plurality of processor functions; and

a system instruction execution unit for selecting one of the plurality of processor functions in response to the system instruction decoded by said system instruction decoder.

21. – 22. (Canceled)

23. (Currently Amended) A processor that performs a first instruction set and a second instruction set, comprising:

a first ~~processing unit that executes processing based on only~~execution controller

executing a first decoded result~~, among a first decoded result and a second decoded result, the first decoded result~~ being a decoded signal of an instruction included in the first instruction set~~,~~;

~~the~~ a second execution controller executing a second decoded result being a decoded signal of an instruction included in the second instruction set~~;~~, the second execution controller being set up independently from the first execution controller;

a first arithmetic unit performing an arithmetical operation relative to execution of only the first decoded result; and

a ~~common processor~~shared arithmetic unit ~~that executes processing based on both the first and second decoded results~~performing an arithmetical operation relative to execution of the first decoded result or the second decoded result.

24. (Previously Presented) The processor according to claim 23, further comprising:

a first decoder that generates the first decoded result by decoding the instruction included in the first instruction set; and

a second decoder that generates the second decoded result by decoding the instruction included in the second instruction set.

25. (Canceled)

26. (Previously Presented) The processor according to claim 23, further comprising:

a common instruction set decoder that decodes a common instruction included commonly in the first and second instruction sets.

27. (Previously Presented) The processor according to claim 24, further comprising:

a pipeline stage that is provided between the first decoder and the first processing unit.

28. (Currently Amended) The processor according to claim ~~25~~24, further comprising:

a first pipeline stage provided between the first decoder and the first processing unit; and

a second pipeline stage provided between the second decoder and the second processing unit.

29. (Previously Presented) The processor according to claim 28, wherein said first pipeline has a different number from said second pipeline.

30. (Previously Presented) The processor according to claim 27, wherein said stage number of the pipeline is variable.

31. (Previously Presented) The processor according to claim 28, wherein the stage number of the first and second pipelines are variable.

32. (Previously Presented) The processor according to claim 24, further comprising a system instruction decoder that decodes a system instruction which selects use of any one of the first and second decoders.

33. (Previously Presented) The processor according to claim 32, wherein said system instruction decoder is provided separate from the first and second decoders.

34. (Previously Presented) The processor according to claim 24, wherein any one of the first and second decoders is selected for use in response to an interrupt signal.

35. (Previously Presented) The processor according to claim 32, wherein said system instruction includes at least one of instructions for setting power voltage and/or operating rate at which the processor operates.

36. (Previously Presented) The processor according to claim 23, further comprising:

a memory that stores both the first and second decoded results.

37. – 40. (Canceled)

41. (New) The processor according to claim 23, further comprising:

a first register file operating with regard to execution of only the first decoded result; and

a shared register file operating with regard to execution of the first decoded result or the second decoded result.

42. (New) The processor according to claim 41, further comprising:

a second arithmetic unit performing an arithmetical operation relative to execution of only the second decoded result; and

a second register file operating with regard to execution of only the second decoded result.

43. (New) A processor comprising:

an arithmetic unit performing an arithmetical operation relative to execution of only a first instruction; and

a shared arithmetic unit performing an arithmetical operation relative to execution of the first instruction or a second instruction, the second instruction being different from the first instruction.

44. (New) The processor according to claim 43, further comprising:

a first register file operating with regard to execution of only the first instruction; and

a shared register file operating with regard to execution of the first instruction or the second instruction.

45. (New) The processor according to claim 44, further comprising:

a second arithmetic unit performing an arithmetical operation relative to execution of only the second instruction; and

a second register file operating with regard to execution of only the second instruction.

46. (New) The processor according to claim 45,

wherein the second arithmetic unit and the second register file are in a deactivated state during execution of the first instruction.